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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,157	03/09/2006	Toshiaki Takenaka	2006-0223A	3496

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EXAMINER	
GOFF II, JOHN L	

ART UNIT	PAPER NUMBER
1791	

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12/30/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,157	TAKENAKA ET AL.	
	Examiner	Art Unit	
	John L. Goff	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 9/8/09. The previous 35 USC 112 rejections have been overcome.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. Claims 1, 3, 4, and 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuhas et al. (U.S. Patent 5,464,658) in view of the admitted prior art (Specification pages 1-4, 8, and 9) and MSU ("Composition of Typical Stainless Steels (ASTM A270)").

Yuhas discloses a method of manufacturing a multi-layer circuit board wherein the core circuit boards having circuit patterns thereon, prepreg bonding sheets, copper foils, and lamination plates all have equivalent thermal expansion coefficients (TECs) to form the board without registration problems. Yuhas teaches forming a laminated structure from core circuit boards, prepreg bonding sheets, and copper foils, sandwiching the layers between a pair of lamination plates, and applying heat and pressure to form the laminated structure (Figures 1 and 2 and Column 1, lines 15-22 and 43-63 and Column 6, lines 24-65 and Column 7, lines 59-61 and Column 8, lines 12-20 and Column 9, lines 26-51 and Column 13, lines 17-25).

Regarding the limitation of "a prepreg sheet having a through-hole filled with conductive paste", it isn't clear that Yuhas expressly discloses prepreg sheets of this type although the particular layers of the multi-layer circuit board are not critical to Yuhas and are chosen as a

function of the end use of the board. The admitted prior art discloses a conventional method of manufacturing a multi-layer circuit board comprising providing a structure including a core circuit board having a circuit pattern thereon and a prepreg sheet having a through-hole filled with conductive paste sandwiched between a pair of metal foils further sandwiched between a pair of lamination plates and applying heat and pressure to form a laminated structure (Figures 6A-6D and Page 3, line 6 to Page 4, line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the particular layers of the multi-layer circuit board in Yuhas those known to form a conventional board in the art as evidenced by the admitted prior art to form a known board without registration problems.

Regarding the limitation of "wherein, a thermal expansion coefficient of the pair of lamination plates is equivalent to a thermal expansion coefficient of the core circuit board" and "wherein the metal foil is made of copper, and the thermal expansion coefficient of the pair of lamination plates is smaller than a thermal expansion coefficient of the metal foil", applicants specification defines the term "equivalent" on page 13, lines 17-20 as "In the description that selecting a lamination plate with a thermal expansion coefficient equivalent to that of a core circuit board, the "equivalent" coefficient means that the thermal expansion coefficient of a lamination plate has a permissible range of ±20 % with respect to that of a core circuit board.". This is the interpretation given the claim. Yuhas teaches the lamination plates, copper foil, and core circuit boards all have equivalent TECs to that of copper foil wherein specifically copper foil has a TEC of 17.4 ppm/^{o}C and the core circuit boards are formed to have TECs of 17.4 ppm/ ^{o}C (Table IV). Yuhas does not specifically teach the TEC of the lamination plates other than to suggest the values are close to copper. However, Yuhas does teach forming the lamination

plates of stainless steel alloy such as 304 or 306. Conventional stainless steel alloy such as 304 or 306 is known to have a TEC of 17 ppm/ °C as evidenced by MSU. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the stainless steel alloy in the lamination plates taught by Yuhas that known as conventional in the art having a TEC of 17 ppm/ °C as evidenced by MSU only the expected results being achieved. Thus, Yuhas as modified teaches the TEC of the lamination plates is equivalent to the TEC of the core circuit board and the copper foil with the TEC of the lamination plates also smaller than the TEC of the copper foil.

Regarding claims 3 and 6, the admitted prior art teaches the core circuit board has four or more layers. The admitted prior art teaches the core circuit board and the prepreg sheet are alternately laminated so as to have two or more layers.

Regarding claims 7 and 8, it was considered conventional in the art to use a buffer material and carrying plate between the lamination plates and the multi-layer board to press the board evenly wherein the use of such a material and plate is evidenced by the admitted prior art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Yuhas as modified a known buffer material and carrying plate as evidenced by the admitted prior art to evenly press the board wherein it would have been further obvious that the plates are formed to have a TEC equal or equivalent to the TEC to the lamination plates as the TECs of all materials are required by Yuhas to be at least equivalent to prevent any registration problems in forming the board. The buffer material is considered capable of accommodating a difference in the thermal expansion of the pair of lamination plates a thermal expansion of the carrying plate.

Regarding claims 4, 9, 10, and 15, Yuhas and the admitted prior art teach the prepreg sheet contains a base and a resin layer impregnated with the base to form a resin layer on both surfaces of the base wherein Yuhas further teaches the prepreg is B-staged in which a woven fabric is impregnated with a thermosetting resin including wherein the fabric has thickness of approximately 70 microns considered after impregnation to have a thickness of approximately 70 microns. Yuhas further teaches forming conventional core circuit boards with a thickness of 0.05 to 1mm, i.e. wherein the core circuit board is not less than one times a thickness of the prepreg sheet.

Regarding claims 11-14, Yuhas as modified measures the TEC of all of the layers including the core circuit board having a predetermined circuit pattern, and the lamination plates are selected equivalent to the measured TEC. Yuhas teaches measuring the TEC at two or more positions of the board considered to include the circuit pattern and in a range from room temperature to a heat pressing temperature using a thermo-mechanical measurement apparatus, and calculates the average TEC for the board.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yuhas, the admitted prior art and MSU as applied above in paragraph 3, and further in view of Ikeguchi et al. (JP 57011026 and see also the abstract).

Yuhas as modified teaches all of the limitations in claim 2 except for a specific teaching that the thickness of the resin layer formed on both sides of the base is at least 20 microns in total thickness, it being noted Yuhas is not limited to any particular thickness. Ikeguchi disclose a prepreg excellent in workability comprising a base and a resin layer impregnated with the base to form a resin layer on both sides of the base having at least 20 microns in total thickness (See the

abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the resin layers on both sides of the base as taught by Yuhas as modified with a thickness at least 20 microns in total as shown by Ikeguchi to form a prepreg excellent in workability.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yuhas, the admitted prior art, and MSU as applied above in paragraph 3, and further in view of Del (U.S. Patent 4,180,608).

Yuhas as modified teaches all of the limitations in claim 15 except for a specific teaching that the thickness of the prepreg after pressing is 60 μm, it being noted Yuhas is not limited to any particular thickness, and Yuhas suggests a fabric thickness before pressing of 86 microns considered approximately 86 microns after impregnation. It is known that a prepreg after pressing results in a reduced thickness, e.g. about 75%, as shown by Del (Column 7, lines 33-35). It would have been obvious to one of ordinary skill in the art at the time the invention that pressing the prepreg sheets taught by Yuhas as modified results in a known expected reduced thickness of about 75% as evidenced by Del.

Response to Arguments

6. Applicant's arguments with respect to claims 1-4 and 6-16 have been considered but are moot in view of the new ground(s) of rejection.

In view of applicants amendment and arguments the previous rejections are withdrawn. The new limitations are fully addressed above.

Applicants argue, "Second, Applicants note that, if the logic that "equivalent" means ±20%, then the term "smaller," as recited in claim 1 should indicate that the thermal expansion coefficients of the core circuit board and the pair of lamination sheets are not equivalent, but are different beyond the of "equivalent." However, page 4 of the Office Action (last paragraph) relies on the permissible range of ±20% for also teaching that the thermal expansion coefficients are different/smaller. The Applicants respectfully disagree, because the definition of "equivalent" cannot be relied upon for teaching both a relationship that is "equivalent," and a relationship that is "different/smaller," as required by claim 1.".

The term "smaller" given its usual definition means less than something else, it being noted applicants do not define "smaller" in the specification rather the term is derived from an example. Thus, "smaller" merely excludes equal to or greater than. Equivalent does not mean equal as evidenced by applicants definition which includes ±20% such that the TEC can be both smaller and equivalent. Newly cited Yuhas meets the claim limitations.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571)272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John L. Goff/
Primary Examiner, Art Unit 1791